Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Q12**
2. **Q13**
3. **Q14**
4. **Q6**
5. **Q5**
6. **Q7**
7. **Q4**
8. **GND**
9. **OSC OUT2**
10. **OSC OUT1**
11. **OSC IN**
12. **MR**
13. **Q9**
14. **Q8**
15. **Q10**
16. **VCC**

**.063”**

**.063”**

**1 16**

**15**

**14**

**13**

**12**

**11**

**8 9 10**

**2**

**3**

**4**

**5**

**6**

**7**

**MASK**

**REF**

**74HC4060**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 74HC4060**

**APPROVED BY: DK DIE SIZE .063” X .063” DATE: 8/26/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HC4060**

**DG 10.1.2**

#### Rev B, 7/1